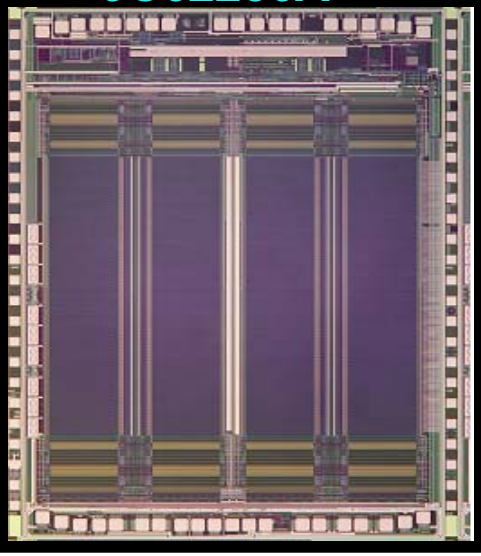
3RD GENERATION MRAM DESIGN

9C62256A



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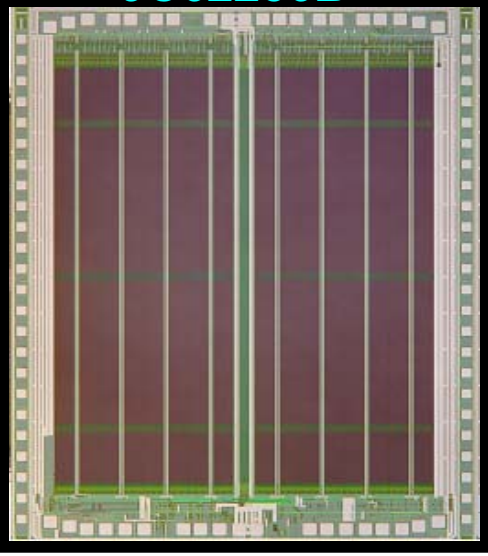

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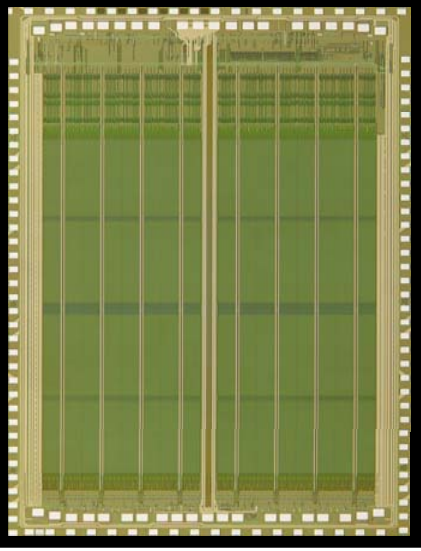

ARCHITECTURE	2T2R (REV A)	3T2R (REV B)	3T2R (REV C)
CELL SIZE	11.5μ²	18.8μ²	24.0μ²
1ST SILICON	7/02	6/03	3/04
DISTURBABLE	YES	NO	NO
CRITICAL CONTROLS	WRITE I DIST DISTURB I DIST X CURRENT / TIME Y CURRENT / TIME	WRITE I DIST _ _ Y CURRENT / TIME	WRITE I DIST _ _ Y CURRENT / TIME
REPAIRABILITY	2 ROWS	4 ROWS	64 SUB ROWS
REDUNDANT LOGIC	LASER FUSE	LASER FUSE	MRAM LATCH