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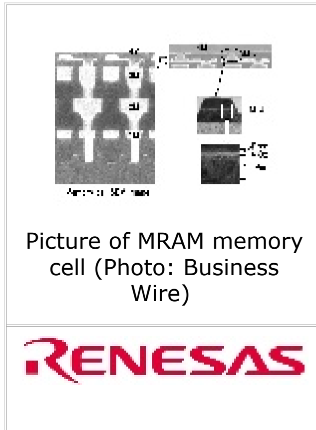
Renesas Technology Develops High-Speed, High-Reliability MRAM Technology

2004 IEEE International Electron Device Meeting



Picture of MRAM memory cell (Photo: Business Wire)

TOKYO & SAN FRANCISCO--(BUSINESS WIRE)--Dec. 14, 2004--

Prospect of High-Speed Operation of over 143 MHz at 1.2 V Operating Voltage and High Reliability of over One Trillion Rewrites

Renesas Technology Corp. today announced the development of a high-speed, high-reliability MRAM (Magnetoresistive Random Access Memory) technology for SoC (system-on-a-chip) use.

Using this technology, Renesas Technology fabricated a prototype 1-Mbit MRAM employing a 130 nm (nanometer) CMOS process. Investigation showed the prospect of high-speed operation with an operating frequency of 143 MHz or above at a 1.2 V operating voltage, and measurements in a one-trillion-rewrites experiment confirmed that there was no degradation.

Renesas Technology achieved these results through joint research with Mitsubishi Electric Corporation, and announced them on December 14 (local time) at the 2004 IEEE International Electron Device Meeting (IEDM) to be held in San Francisco from December 13.

Background

The functions and performance of mobile devices and digital consumer appliances have improved remarkably in recent years, and this trend will continue in the future. As higher performance and functionality, lower power consumption are required in product development, there is a demand for technologies that will make this possible.

Memory elements used for data storage and others play an important role as a key technology supporting higher product functionality and performance, and various types of memory elements have been developed to date. To meet future needs, efforts are being made to improve various kinds of conventional volatile and nonvolatile memory elements on the one hand, at the same time as research is being conducted into new types of next-generation memory offering novel characteristics.

One such new kind of memory, MRAM, is nonvolatile memory that enables data to be retained when power is cut while also providing high-speed operation capability. This ability to implement functions provided by various kinds of conventional memory has led to high expectations of MRAM as next-generation memory.

Details of the Technology

Details of the newly developed technology are as follows.

(1) Establishment of an optimization method for realizing maximum performance

MRAM stores data by using magnetic material often used in hard disk read magnetic heads, and an MTJ

(Magnetic Tunnel Junction), which comprises a tunnel layer. Its performance depends on the composition and structure of this MTJ. The joint development team looked at the relationship between the magneto-resistance (MR) ratio(*1) and resistance-area (RA)(*2) in the MTJ, and by further applying correlativity with read speed, the team established an original method of finding the optimal conditions for achieving high speed.

This optimization method was developed ahead of other manufacturers, and was established by making clear the universal relationship that exists between electrical resistance and the magneto-resistance ratio. Use of this method makes it possible to determine the best combination of electrical resistance and magneto-resistance ratio.

(2) Use of magnetic material enabling high speed plus tunnel layer optimization

The MTJ structure comprises a free layer, tunnel layer, and pin layer. With conventional Renesas MRAM, CoFe (ferrocobalt: magnetic material), AlOx (alumina), and CoFe are used respectively, and high-speed operation with an operating frequency exceeding 100 MHz has been confirmed in trial production.

In order to attain still higher speed, it is necessary to achieve a higher magneto-resistance ratio, but investigation with the optimization method showed that it is difficult to improve the magneto-resistance ratio with CoFe. For this reason, the following techniques were studied and applied in order to achieve higher speed.

(a) Use of CoFeB (ferrocobalt boron) as magnetic material

With the above optimization method, material-related studies can be conducted simultaneously. As a result, it was found at the same time that CoFeB rather than CoFe is suitable for realizing a magneto-resistance ratio that enables high-speed operation. As predicted by the optimization method, the use of CoFeB improved the magneto-resistance ratio by approximately 30% to 70%.

(b) Optimization of tunnel layer thickness

Although simply changing the magnetic material to CoFeB increases the magneto-resistance ratio, electrical resistance also increases, and higher speed cannot be achieved. On the other hand, electrical resistance can be lowered by making the tunnel layer thinner, but an excessively thin tunnel layer leads to reliability problems. Using the present optimization method, the development team found the right tunnel layer thickness that enables both high speed and reliability. This has made it possible to realize a high magneto-resistance ratio and low electrical resistance at the same time.

Use of the above approach gives a cell sensing time (data read time) of 5.2 ns, presenting the prospect of achieving a read cycle of approximately 7 ns and an operating frequency in excess of 143 MHz. Furthermore, an experiment in which one trillion write cycles were executed in a high-temperature environment of 150 degrees C showed almost no degradation. This confirmed that high reliability can be achieved despite reducing the thickness of the tunnel layer.

Effects of the New Technology

Using the technology, a prototype MRAM was fabricated using 4-layer Cu wiring, and its effects were studied. Using a 1T-1MTJ structure comprising one transistor and one MTJ for the memory cells, a TMR (tunnel magneto-resistance) element size of 0.26 x 0.44 um2 and the world's smallest memory cell size of 0.81 um2 were achieved.

About Renesas Technology Corp.

Renesas Technology Corp. designs and manufactures highly integrated semiconductor system solutions for mobile, automotive and PC/AV markets. Established on April 1, 2003 as a joint venture between Hitachi, Ltd. (TSE:6501) (NYSE:HIT) and Mitsubishi Electric Corporation (TSE:6503) and headquartered in Tokyo, Japan, Renesas Technology is one of the largest semiconductor companies in the world and world leading microcontroller supplier globally. Besides microcontrollers, Renesas Technology offers system-on-chip devices, Smart Card ICs, mixed-signal products, flash memories, SRAMs and more.

http://www.renesas.com

Notes:

1. Magneto-resistance ratio: In MRAM, 0 and 1 data are determined by a high and low resistance respectively. Magneto-resistance ratio is a ratio in which the low resistance value is the denominator and the resistance difference (high resistance value -- low resistance value) is the numerator. As the magneto-resistance ratio increases, erroneous operations during reading decrease, enabling operating speed to be increased.

2. Electrical resistance: A quantity whereby the lower resistance is normalized for the MTJ area in the two MRAM states.

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