Magneto-Resistive IC Memory Limitations and Architecture Implications

Roy E. Scheuerlein
IBM Almaden Research Center
650 Harry Road, San Jose CA 95120
rscheue@us.ibm.com, 408-927-3844

Abstract

Magneto Resistive, MR, elements offer an alternative approach to non-volatile VLSI memory. The approach has unique aspects which will be related to the requirements of high speed, dense, deep sub-micron VLSI memory. The limitation of resistor thermal noise, sensing power, write current, switch fan out, bandwidth, and voltage supply are discussed. Possible MRAM array architectures are listed in the first section. A novel architecture called the Cross Point MTJ MRAM is described that potentially offers higher signal to noise ratio, lower power and higher density than the alternatives. In following sections Signal to Noise Ratio (SNR) and Power Versus Bandwidth constraint equations are proposed for MRAM architectures. Sensing alternatives for MR elements are reviewed and voltage requirements of MRAM architectures are described. Finally MRAM alternatives are compared.

Introduction

The role of MRAM in the crowded arena of VLSI memories is not yet clear. Success as a small niche market depends on superiority of perhaps a single charateristic such as durability in hostile environments. But sucess as a major VLSI memory segment probably requires a combination of nonvolatility, high density, high performance, and low power dissipation. DRAM excells in the area of high density at low cost and low power dissipation. SRAM excells in high performance and low power dissipation. Flash provides nonvolatility at high density. FeRAM has had some success providing nonvolatility at modest density levels and modest performance levels. This paper investigates the potential of MRAM architectures to achieve a compelling combination of the desired features.

The next section summarises the key features of MRAM architectures.

MRAM Architectures

Early MRAM designs took advantage of the Anisotropic Magneto Resistance AMR effect. In order to achieve high density, MRAM architectures must provide a small cell size. In terms of the average feature size λ, DRAM cells which use a folded bit line architecture occupy 8 λ^2. The series AMR cell proposed for high density MRAM [1] elongates the MR element by 4 to 1 to achieve resistance values compatible with VLSI circuits and has a cell area about 12 λ^2. The usable AMR effect in memory cells is about 2%. Because there is no cell selection device, a crossing word line is used to disturb the selected resistor during sensing opperations. The disturb could be destructive or non-destructive to the memory state. Conveniently the sense and word lines can also be used to write a unique cell in the array.

Giant Magneto Resistance GMR providing a MR ratio of about 6% improves MRAM SNR and performance. The GMR MRAM architecture is also a series string of N resistors [2]. Due to structure and resistance similarities to AMR, the cell size is also about 12 λ^2. A Pseudo Spin Valve PSV sensing mode [3],[4] doubles the signal provided by the GMR device but leads to higher write currents since the data is stored in the harder of the two ferromagnetic layers. A word line is provided to disturb the cell during sensing. Since the orientation of the magnetization for the data state in GMR cells is parallel to the sense line, an extra write conductor is included in the cell for writing [3].

Tunnel Magneto Resistance TMR promises even higher MR ratios [5] and has high resistance and a vertical sensing current direction which allows alternative architectures for MRAM arrays. The SNR of either serial or parallel resistors can be expressed as:

SNR=Vo MR / (4kT N Rm BW)* * 1/2

SNR would tend to decrease for the TMR architectures due to the high resistance Rm of the TMR devices. This is mitigated by the higher Vo bias across the element, and higher MR ratio. An example calculations for a TMR resistor value of 10 KΩ, TMR ratio of 15% at 300 mv bias, N of 32, and a bandwidth BW of 100 Mhz gives a satisfactory SNR of 62 assuming Johnson Noise. TMR devices in the submicron size range will require perfecting lower specific resistance magnetic tunnel junctions.

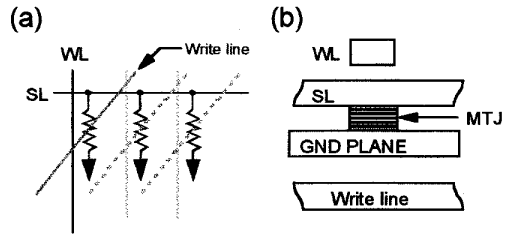


Figure 1) Parallel TMR MRAM (a) Circuit, (b) Cross section.

A parallel arrangement of resistors, Fig. 1, is suggested by the high resistance value. In this arrangement the voltage required in the array can be reduced by a factor N from the series arrangement while providing the same signal voltage. The TMR devics is implemented as a vertical stack of a lower electrode, a very thin tunnel barrier and an upper electrode comprising a Magnetic Tunnel Junction MTJ. A word line WL not connected to the MTJ is required for sensing, which could be either PSV mode or destructive read mode. Since the MTJ can be damaged by voltages about one volt, and the parallel combination of MTJs would shunt write currents, a separate write conductor is needed. A write conductor path diagonally across the array is the most area efficient. A

planarization processes [6] to passivate the MTJ allows borderless contact of the top conductor to the MTJ making a 7 λ^2 cell possible, Fig. 2. Dissadvantages include the large spacing of the write conductors to the ferromagnetic layers and the need for three lines plus a ground connection per cell.

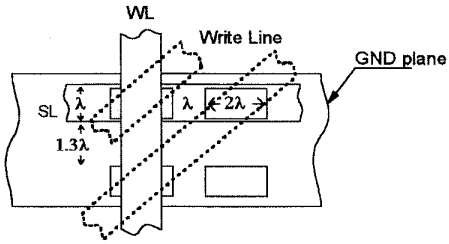


Figure 2) Parallel TMR Layout $7\lambda^2$

A matrix arrangement, Fig. 3, of TMR elements is also possible. In this case the electrodes of the MTJ are connected to two sense line, SLx and Sly. SLy is selectively connected to ground to complete the sense path. The matrix of unselected MTJs in an N by N arrangement of cells is equivalent to N/2 parallel resistors, so this arrangement has slightly better SNR than parallel or series arrangements. In arrays sizes of interest, pattern sensitivity to the sneak paths will require a word line to facilitate PSV or destructive read mode sensing. An extra line for write currents is also required so there are a total of four lines per cell. Since the bottom electrode typically overlaps the MTJ, the cell size is 9 λ^2.

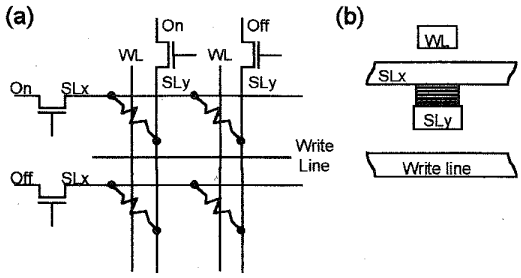


Figure 3) Matrix TMR MRAM (a) Circuit, (b) Cross Section

A switch plus TMR cell is also possible because TMR resistance is compatible with FET switch impedance levels. The word line controls the switch which causes the sense path to go through only a single TMR element. Therefore signal increases by a factor of N and SNR increases by a factor of square root of N. Since the switch can be off when writing the cell, the sense line SL connected to the top electrode of the MTJ can carry write currents. A third line carries the other write current and can also provide a ground connection during sensing. The cell is estimated to be 12 λ^2 because of the switch area.

Cross Point MTJ Architecture

A final TMR arrangement, called the Cross Point MTJ Architecture [7] shown in Fig. 4, uses a diode to block the sneak paths in a matrix arrangement. Each cell has a MTJ and a diode in series between two metal lines at their cross point. The cell is selected by grounding one word line, while the other word lines are as high as the sense line. The sense curent goes through the one diode that is forward biased. The same two lines can be used for the write currents because the voltage drop of the diode protects the MTJ from write curent induced IR drops. The close proximity of the conductors to the MTJ reduces the write currents required. In addition the RC time constants on the array lines are determined by the capacitance of the diode rather than the high capacitance of the tunnel junction reducing sensing time compared to parallel or matrix TMR arrangements.

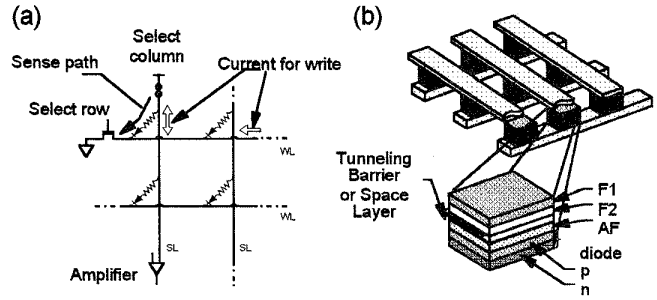


Figure 4) Cross Point MTJ MRAM (a) Circuit, (b) Structure

The cell requires a thin film diode integrated with VLSI metalization and MTJ processes which is a significant challenge. The cell size is estimated to be 9 λ^2 or as small as 6 λ^2, Fig. 5, depending on achieving borderless contacts to the diode.

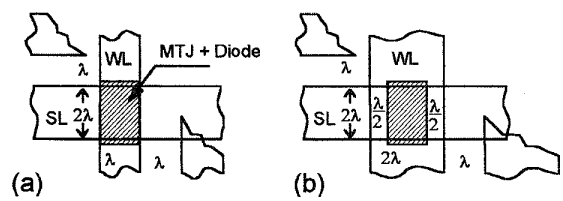


Figure 5) Cross Point MTJ MRAM Layout (a) $6\lambda^2$, (b) $9\lambda^2$

Diode Requirements

The ideality factor of the diode effects the differential resistance of the diode which must be smaller than the resistance of the MR element. This requirement implies that the IR drop across the TMR device must be greater than the ideality factor times the diode thermal voltage. The falloff of TMR to half its maximum occurs at a bias voltage in the range of hundreds of millivolts [6] therefore many times the thermal voltage of the diode. The requirement regarding the diode differential resistance therefore can be met without significant MR rolloff.

Since it provides isolation of the sense path from sneak paths through the unselected cells, the diode for the cross point MTJ array must have an on to off conductance ratio in the range of four orders of magnitude for arrays 128 by 128 bits. The reverse bias on the unselected cells can be less than one volt. Conductance ratios this large are achievable with

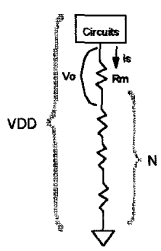
thin film diodes. However the on conductance of typical thin film material is too low for cells with feature sizes less than a micron. Improved mobility thin film material would be required to implement Cross Point MTJ cells.

Signal versus Power

An equation relating signal to sense power in terms of SNR, the resistance of the element, and MR ratio is shown in Fig. 6. Small N, high resistance, and high MR reduce sense power. An alternate expression, in terms of Vo, is the same for all the MR architectures: $Ps \geq N\,(Vo)^2 / Rm$, where N is the number of equivalent series or parallel resistors in the sense path. Matrix arrangements of N by N have (N+1)/2 equivalent parallel paths. Series GMR and Parallel TMR have similar sense power because both Vo and Rm increase substantially for TMR. However, the switched TMR architectures will have four orders of magnitude lower sense power than series GMR because all factors in the equation in Fig. 6 improve: N is one, Rm is 100 times and MR is three times larger.

$$\boxed{Ps \geq \frac{N}{Rm}(Vo)^2} = \frac{N}{Rm}(Vsig)^2\left(\frac{1}{MR}\right)^2 \quad \text{(For Series R)}$$

$$= \frac{N}{Rm}(N\,Vsig)^2\left(\frac{1}{MR}\right)^2 \quad \text{(For Parallel R)}$$



$$Ps \geq (N\,Vo\,Is) \text{ and } Is = \frac{Vo}{Rm}$$

$$Vsig = (Vo)(MR) \longrightarrow Vo = \frac{Vsig}{MR}$$

$$Ps = (N\,Vo)(Vo/Rm = \frac{N}{Rm}(Vo)^2 = \frac{N}{Rm}\frac{Vsig^2}{MR^2}$$

Figure 6) Sense Power vs. Signal

Power versus Bandwidth Constraint

The signal versus power expression can be combined with the SNR constraint to eliminate most variables and create a fundamental constraint on MRAM power versus BW.

Bandwidth is a key requirement. It depends on the application and increases rapidly in succeeding memory technology generations. A fundamental constraint equation relating sensing power, bandwidth, signal to noise ratio and MR ratio is shown in Fig.7. It is applicable to the sensing of resistors organized in all the different arrangements. This equation indicates that the number N of magneto resistor elements in series with the sensing circuitry impact the fundamental constraint proportional to N squared.

For Series R

$$SNR = \frac{Vsig}{\sqrt{4kT\,N\,Rm\,BW}}$$

$$Vsig^2 = (SNR)^2\,4kT\,N\,Rm\,BW$$

$$Ps \geq \frac{N}{Rm}\frac{(SNR)^2\,4kT\,N\,Rm}{(MR)^2}(BW)$$

$$\boxed{\frac{Ps}{BW} \propto \frac{N^2}{(MR)^2}(SNR)^2}$$

For Parallel R

$$SNR = \frac{N\,Vsig}{\sqrt{4kT\,N\,Rm\,BW}}$$

$$(N \cdot Vsig)^2 = (SNR)^2\,4kT\,N\,Rm\,BW$$

$$Ps \geq \frac{N}{Rm}\frac{(N \cdot Vsig)^2}{(MR)^2}(BW)$$

$$Ps \geq \frac{N}{Rm}\frac{(SNR)^2\,4kT\,N\,Rm}{(MR)^2}(BW)$$

Figure 7) Power Bandwidth Ratio for MRAM

Sensing Techniques

Various sensing approaches have been proposed for magneto resistive memory. Auto zero sensing involves a self-reference to the MR element requiring additional sensing time. PSV technique also involves a self-reference to the MR element and auto zero sensing. In addition destructive readout techniques require longer cycle times to restore data. All these approaches will be considerably slower than the direct sensing used in DRAM and Flash memories. It is possible to consider direct sensing for MR cells in the case of switched MR cells which give large signal levels if the tracking of resistance value between MR elements is less than the MR ratio. The Cross Point MTJ cell could be operated in a twin cell arrangemant where two adjacent cells are always writen to opposite states and then connected to opposite sides of the sense amplifier for sensing. If the tracking of adjacent MR elements is less than the MR ratio, the data state will be indicated by the remaining signal. Of course a bit would occupy twice the area, but the memory performance in terms of cycle time could be faster than DRAM since this is a nondestructive sensing scheme.

Array Efficiency

For efficient VLSI memory chips, the switches used to drive the lines that access the array of cells need to service a large fan out of cells. Bi-directional switches are needed for the write lines. The requirements of selection devices in different cell arrangement and the area implication of selection devices is summarized in Fig. 8. Serial and parallel architectures all contain at least four switches to control the lines for a given cell. The effect of non-rectangular arrays typically used because the signal can be improved at a small cost in selection devices is included. If bi-directional currents which require two switches per line are only placed on the long lines, a significant area savings can result. However, the IR drop in the write lines for MRAM arrays is a critical limitation to scaling to multi-megabit memories. The switches in the cell of TMR architectures are assumed to be equivalent to one eigth the peripheral switches, since only the sense current which is less than 100 μA must be conducted.

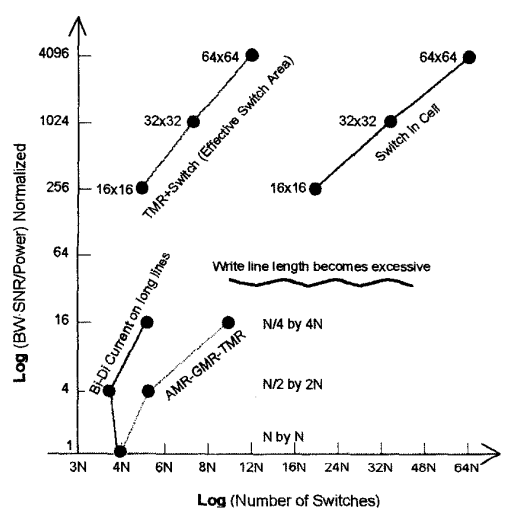


Figure 8) Power Bandwidth Ratio for MRAM vs. Switch Count

Comparison of MRAM Alternatives

To compare MRAM architectures, Table 1 summarizes cell area estimates, SNR, the ratio of Bandwidth times SNR to Sense Power, and number of lines required to control the cell to indicate cell complexity. Only the switched TMR are seen to be competitive with DRAM. Others fall far short in regard to SNR and sense power.

Table 2 compares design points for series GMR, parallel TMR and a switched TMR architecture. The switched TMR is shown to have dramatically higher SNR and lower sense power.

Conclusions

A fundamental constraint equation considering SNR, BW and sense power indicates that the number of MR elements in series with the sensing circuitry impact the fundamental constraint proportional to the number squared. It is unlikely that traditional MR architectures can achive a desired combination of high performance, low power and high density for multi-megabit memories because of this constraint. Switched TMR architectures have four orders of magnitude lower sense power at the same signal level, and four orders of magnitude advantage in the power versus bandwidth constraint equation compared to MRAM arrays with N equal to 32. This provides a route to simultaneously achieve high signal level for high performance, low sense power and small cell size in an MRAM design. Switched TMR architectures are a potential approach for MRAM to achieve multi-megabit memories, assuming significant technology hurdles in magnetic tunnel junctions can be overcome.

Acknowledgments

Many useful discussions with Dr. W. J. Gallagher, and Dr. S. S. Parkin of IBM Research are gratefully acknowledged.

References

1. Pohm, A.V. et al, "The Design of a One Megabit Non-volatile M-R Memory Chip Using 1.5 x 5 μm Cells," IEEE Trans. on Magnetics, Vol. 24, No. 6 (Nov. 1988), pp. 3117-3119.
2. Tang, D. D. et al, "Spin-Valve RAM Cell," IEEE Trans. on Magnetics, Vol. 31 (Nov. 1995), pp. 3206-3208.
3. Pohm, A. V. et al, "Experimental and Analytical Properties of 0.2 Micron Wide, Multi-layer, GMR, Memory Elements," IEEE Trans. on Magnetics, Vol. 32, No. 5 (Sept. 1996), pp. 4645-4647.
4. Daughton, J. M., "Magnetic Tunneling applied to Memory," 41st Annual Conference on Magnetism and Magnetic Materials, Paper AA-04, November 12, 1996.
5. Gallagher, W. J. et al, "Microstructured Magnetic Tunnel Junctions," J. Applied Physics, Vol. 81, No. 8 (April 1997), pp. 3741-3746.
6. Lu, Y. et al, "Bias Voltage and Temperature Dependance of Magnetic Tunnel Junctions," J. Applied Physics, Vol. 83, No. 11 (June 1998), p. 6515.
7. W. Gallagher, J. Kaufman, S. Parkin, R. Scheuerlein, U.S.P. 5,640,343, June 1997.

Table 1) *MRAM architecture comparison of area, SNR, sense power, and complexity, assuming TMR = 15%, GMR = 6%, AMR = 2%, Rm = 10 KΩ for TRM and 100 Ω for GMR and AMR. The SNR is for 100 Mhz, and noise factor of one. The DRAM SNR, estimated for the cell switch, is not the limiting factor because of non-random coupled noise sources.*

	Area	SNR	4kT BW SNR ^{2} ÷ Ps	Lines Per Cell
Serial AMR	$12\,\lambda^2$	$6 \bullet \sqrt{64/N}$	MR^2 / N^2	2
Serial GMR	$12\,\lambda^2$	$17 \bullet \sqrt{64/N}$	MR^2 / N^2	3
PSV GMR	$12\,\lambda^2$	$35 \bullet \sqrt{64/N}$	$4\,MR^2 / N^2$	3
Parallel TMR	$7\,\lambda^2$	$44 \bullet \sqrt{64/N}$	MR^2 / N^2	3+gnd
Matrix TMR	6 to $9\,\lambda^2$	$62 \bullet \sqrt{64/N}$	$2\,MR^2 / N^2$	4
Switch+TMR	$12\,\lambda^2$	348	MR^2	3
Diode+TMR	6 to $9\,\lambda^2$	300	$\cong MR^2$	2
DRAM	$8\,\lambda^2$	200 - 400	0.1 - 0.4	3+gnd

Table 2) *MRAM Design Point Comparison for GMR, Parallel TMR and Diode TMR architectures at 2.5 v, 0.5 micron technology.*

	Series GMR	Parallel TMR	Crosspoint MTJ
N	32	32	1
MR	6%	15% at .3v	15% at .3v
Rm	100 Ω	10k Ω	10k Ω
Vsig	3.0 mV	1.4 mV	45 mV
Vo	50 mV	300 mV	300 mV
Array Voltage	1.6 V	300 mV	Vo+Vdiode
Cell Ps	0.8 mW	0.3 mW	9 μW
Ps	1.25 mW	2.4 mW	75 μW
SNR at 100 MHz	41	62	348 • (Rm/Rm+Rd)
Concerns	Vdd Scaling Power Low Rm	TMR Rolloff Power High Rm	Thin Film Diode