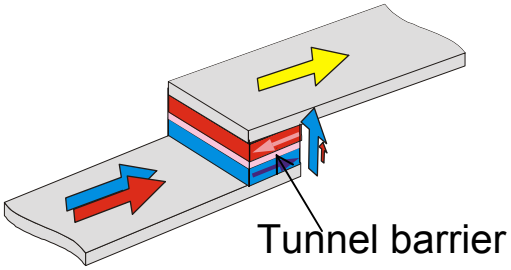
History of MTJ MRAM Developments



1974 Slonczewski (IBM) – MTJ concept proposed (internally in IBM)

1975: Juliere (CNR-France) - first MTJ demonstration

Fe/Ge/Co, $\Delta R/R$~14% at 4.2 K

1982: Maekawa and Gafvert (IBM) – MTJ demonstration

Ni/NiO/Ni, Fe, Co, $\Delta R/R$~0.4-2% at 4.2 K

1990~1993: Miyazaki et al. (Tohoku University) -- MTJ demonstration

NiFe/Al-Al_2O_3/Co, $\Delta R/R$~2.7% at room temperature

1995: Miyazaki et al. (Tohoku University) - first large room temperature MR

Fe/Al-Al_2O_3/Co, $\Delta R/R$~18% at room temperature

1995: Moodera et al. (MIT) - large room temperature MR

Co-Fe/Al-Al_2O_3/Co, $\Delta R/R$~10% at room temperature

1996: Parkin et al. (IBM) - large room temperature MR

>25% in shadow masked and patterned junctions; reproducible

1998: Parkin et al. (IBM) - extraordinarily large room temperature MR; high thermal stability

>35% in sub-micron junctions; >47% in shadow masked junctions

specific resistances ~60 to >10^9 $\Omega(\mu m)^2$; thermal stability (>300 °C)

1999-2000: Scheuerlein et al. (IBM) 1st MTJ MRAM demonstration, <3 ns read and write

2002 Durlam et al. (Motorola) - 1Mbit MRAM in 0.6μm technology

2003 Sitaram et al.; Bette et al. (IBM & Infineon) - 128kbit MRAM core in 0.18μm technology

2003 Durlam et al. (Motorola) – 4 Mbit MRAM in 0.18μm technology, toggle write; product sampling

2004 Debrosse et al. (IBM & Infineon) – 16Mb MRAM (accepted for Symposium VLSI Circuits)