Session 23: Integrated Circuits and Manufacturing – Non-Volatile Memory Technology; MRAM, RRAM and FeRAM

Tuesday, December 14, 2:15 p.m.
Imperial Room A

Co-Chairs: Iwao Kunishima, Toshiba
Atsushi Hori, Matsushita

2:15 p.m.
Introduction

2:20 p.m.
23.1 Status and Outlook of Emerging Nonvolatile Memory Technologies, G. Mueller, T. Happ, M. Kund, G.Y. Lee, N. Nagel, and R. Sezi, Infineon Technologies, Munich, Germany

This paper reviews the concept, status and challenges of emerging nonvolatile memory technologies. The technologies that are discussed and compared to state of the art Flash technology are the Conductive Bridging RAM, the Ferro-electric RAM, the Magneto-resistive RAM, the Organic RAM and the Phase Change RAM.

2:45 p.m.
23.2 Design and Process Integration for High-Density, High-Speed, and Low-Power $6F^2$ Cross Point Type MRAM Cell, Y. Asao, T. Kajiyama, Y. Fukuzumi, M. Amano, H. Aikawa, T. Ueda, T. Kishi, S. Ikegawa, K. Tsuchida, Y. Iwata, K. Shimura*, Y. Kato*, S. Miura*, N. Ishiwata*, H. Hada*, S. Tahara*, and H. Yoda, Toshiba Corporation, Kawasaki, Kanagawa, Japan, *NEC Corporation, Kanagawa, Japan

A new cross point type cell was proposed for high-density of $6F^2$, high-speed, and low-power MRAM. A 1Mb chip was fabricated utilizing 0.13µm CMOS and 0.24 X 0.48μm^2 MTJ sandwiched with the efficient yoke wires. The access time of 250ns and 1.5V operations were demonstrated with the 1Mb chip.

3:10 p.m.
23.3 High Density and Low Power Design of MRAM, C. C. Hung, M. J. Kao, Y. H. Chen, Y. H. Wang, H. H. Hsu, C. M. Chen, Y. J. Lee, W. C. Chen, W. C. Lin*, K. H. Shen, J. H. Wei, L. C. Wang, K. L. Chen, S. Chao**, D. Tang*, M.-J. Tsai, ERSO ITRI, Hsinchu, Taiwan, ROC, *TSMC, Hsinchu, Taiwan, ROC, **National Tsing Hua University, Hsinchu, Taiwan, ROC

Novel MRAM structures based on 1T2UMTJ cell and PWWL architecture are proposed to shrink the bit size with a potential down to 6 F2 by a so-called ExtVia process and reduce the writing current by a factor of two, making the MRAM suitable for universal memory applications.

3:35 p.m.
23.4 A 0.13µm MRAM with 0.26x0.44µm2 MTJ Optimized on Universal MR-RA Relation for 1.2V High Speed Operation Beyond 143MHz, S. Ueno, T. Eimori, T. Kuroiwa*, H. Furuta, J. Tsuchimoto, S. Maejima, S. Iida, H. Ohshita, S. Hasegawa, S. Hirano, T. Yamaguchi, H. Kurisu, A. Yutani, N. Hashikawa, H. Maeda, Y. Ogawa, K. Kawabata, Y. Okumura, T. Tsuji, J. Ohtani, T. Tanizaki, Y. Yamaguchi, T. Ohishi, H. Hidaka, T. Takenaga*, S. Beysen*, H. Kobayashi*, T. Oomori*, T. Koga and Y. Ohji, Renesas Technology Corporation, Itami, Hyogo, Japan, *Mitsubishi Electric Corporation, Hyogo, Japan

A 0.13µm Magnetoresistive Random Access Memory (MRAM) with 0.26x0.44µm2 Magnetic-Tunneling-Junction (MTJ) is presented for 1.2V high-speed operation beyond 143MHz, where MTJ parameters are best-tuned for its maximum performance. We have found that there is a universal relationship between magneto-resistance (MR) and resistance-area (RA) for MTJs with CoFe/AlO_x material system, and the universality is extrapolated upwards by CoFeB/AlOx material system. Best MR-RA combination is realized on this universality. A 5.2ns sensing is demonstrated by a 0.13µm MRAM with optimized MTJ. This advanced MRAM also shows good reliability for endurance/retention characteristics and strong access immunity in high temperature up to 150°C.

4:00 p.m.
23.5 Improvement of Robustness Against Write Disturbance by Novel Cell Design for High Density MRAM, T. Kai, M. Yoshikawa, M. Nakayama, Y. Fukuzumi, T. Nagase, E. Kitagawa, T. Ueda, T. Kishi, S. Ikegawa, Y. Asao, K. Tsuchida, H. Yoda, N. Ishiwata*, H. Hada* and S. Tahara*, Toshiba Corporation, Kawasaki, Kanagawa, Japan, *NEC Corporation, Kawasaki, Japan

A new bit cell to have an excellent astroid is presented from viewpoints of both theory and experiment. The switching mechanism is unique. The robustness against the disturbance of half selected bits is improved. Its excellent astroid improves thermal stability and gives a potential to achieve extremely high density MRAM.

4:25 p.m.
23.6 Highly Scalable Non-volatile Resistive Memory Using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses, I. G. Baek, M. S. Lee, S. O. Park, H. S. Kim, U.-I. Chung, S. Seo, M. J. Lee, D. H. Seo, D.-S. Suh, J. C. Park, I. K. Yoo, and J. T. Moon, Samsung Electronics Co., Ltd., Kyeonggi-Do, Korea

Simple binary-Oxide Resistive Random Access Memory (OxRRAM) has been fully integrated with 0.18mm technology. OxRRAM is highly compatible with conventional CMOS processes, and shows size independent properties promising high scalability. Excellent high temperature performance and operation condition below 3V, 2mA have been confirmed at a 0.3x0.7mm^2 TMO cell size.

4:50 p.m.
23.7 Fully Logic Compatible (1.6V Vcc, 2 Additional FRAM Masks) Highly Reliable Sub $10F^2$ Embedded FRAM,J.H. Park, H.J. Joo, S. K. Kang, Y. M. Kang, H.S. Rhie, B.J. Koo, S. Y. Lee, B.J. Bae,J.E. Lim, H. S. Jeong and K. Kim, Samsung Electronics Co. Ltd., Kyungki-Do, Korea

We developed a 1.6V operational 1T1C, COB, sub $10F^2$ cell embedded FRAM technologies using a novel 100 nm thick MOCVD PZT

technology and direct cell via technology. A highly reliable PZT capacitor was obtained using a PTO seeding technology. Capacitor degradation was completely prevented by combining a TiN/W-plug scheme and a plate line barrier metal technology. High reliability and 1.6 V low voltage operation has been successfully demonstrated.